AMENDMENTS TO THE CLAIMS

Please amend Claims 1, 6, and 11 as follows, without prejudice or disclaimer to continued examination on the merits:

1. (Currently Amended): A method for connecting data lines, the method comprising:

(a) connecting a switch element, and providing a five-stage logical model that represents the components of the switch element in five stages comprising an input sorter, an input router, a center stage device, an output router, and an output sorter, to a first set of data lines and to a second set of data lines;

(b) identifying a first plurality of time slots on an ingress stage of the switch element;

(c) identifying a second plurality of time slots on an egress stage of the switch element;

(d) assigning each time slot on the ingress stage to a corresponding ingress edge on a center stage of the switch element;

(e) assigning each time slot on the egress stage to a corresponding egress edge on the center stage of the switch element;

(f) assigning each time slot on the ingress stage to a corresponding time slot on the egress stage; and

(g) sending communications from the first set of data lines to the second set of data lines by assigning time slots of the communications individually from the first plurality of time slots through corresponding ingress and egress edges of the center stage and to corresponding time slots in the second plurality of time slots.

2. (Original): The method of claim 1, further comprising clearing all existing traffic on the switch element before assigning each time slot on the ingress stage to a corresponding time slot on the egress stage.

3. (Original): The method of claim 1, further comprising structuring the switch element so that a number of time slots on the ingress side is equal to a number of time slots on the egress side.

4. (Original): The method of claim 1, wherein step (f) includes assigning only one time slot on the egress stage to only one time slot on the ingress stage.

5. (Original): The method of claim 1, wherein prior to performing steps (d)-(g), the method includes detecting a switching event that causes all data carried on the first set of data lines and on the second set of data lines to be destroyed.

6. (Currently Amended): A method for connecting data lines, the method comprising:

establishing a configuration for a switch element, and providing a five-stage logical model that represents the components of the switch element in five stages comprising an input sorter, an input router, a center stage device, an output router, and an output sorter, the switch element including a set of ingress devices, a set of center stage devices, and a set of egress devices, wherein each ingress devices includes multiple ingress routers, and each egress device includes multiple egress routers;

assigning each ingress router multiple time slots from only one data line in the first plurality of data lines;

assigning each egress router multiple time slots from only one data line in the second plurality of data lines;

assigning each router of each ingress device to one router of one of the egress devices, so that each egress router is assigned only one ingress router;

assigning each time slot of each ingress router to one time slot of the egress router assigned to that ingress device; and

establishing a plurality of connections between the first plurality of data lines and the second plurality of data lines using the time slot of each ingress router and each egress router, each connection including one of the ingress devices, one of the center stage devices, and one of the egress devices.

7. (Original): The method of claim 6, wherein a size of each ingress router is equal to the number of center stage devices.

8. (Original): The method of claim 6, wherein a size of each egress router is equal to the number of center stage devices in the switch element.

9. (Original): The method of claim 6, wherein assigning each ingress router multiple time slots from only one data line in the first plurality of data lines includes assigning one or more of the data lines in the first plurality of data lines multiple ingress routers.

10. (Original): The method of claim 6, wherein assigning each egress router multiple time slots from only one data line in the second plurality of data lines includes assigning one or more of the data lines in the second plurality of data lines multiple egress routers.

11. (Currently Amended): A switch element comprising:

a first ingress device, wherein the first ingress device comprises a logical model of an input sorter and a plurality of input routers, providing a first plurality of ingress time slots, the first ingress device connecting to a set of ingress lines;

a center stage device including a plurality of ingress edges and a plurality of egress edges~~,~~;

~~the~~ a first egress device connecting to a set of egress lines~~,; a first egress device~~ wherein the first egress device comprises a logical model of an output sorter and a plurality of output routers, providing a first plurality of egress time slots; and

a processor, providing a five-stage logical model that represents the components of the switch element in five stages comprising the input sorter, the plurality of input routers, the center stage device, the plurality of output routers, and the output sorter, configured to assign each time slot in the first plurality of ingress time slots to an ingress edge in one of the center stage devices, to an egress edge in the one of the center stage devices, and to a corresponding time slot in the first plurality of egress time slots, so that a communication from one of the set of ingress lines is sent to one of the set of egress lines over one of the time slots in the first plurality of ingress time slots, one of the ingress edges and one of the egress edges on one of the center stage devices, and one of the egress time slot.

12. (Original): The switch element of claim 11, wherein the processor is configured to assign multiple ingress time slots to each data line in the set of ingress data lines, and to assign multiple egress time slots to each data line in the set of egress lines, so that each center stage device receives at least one time slot from each data line in the set of ingress data lines, and communicates to at least one data line in the set of egress lines through at least one time slot from that data line in the set of egress lines.

13. (Original): The switch element of claim 11, further comprising a first plurality of ingress devices and a first plurality of egress devices, wherein the processor is configured to assign one or more data lines in the set of ingress data lines to each ingress device in the plurality of ingress devices, and one or more data lines in the set of egress data lines to each egress device in the plurality of egress devices, so that a plurality of ingress time slots provided by each data line in the set of ingress lines are assigned to only one ingress device and to each center stage device, and so that a plurality of egress time slots provided by each data line in the set of egress lines are assigned to only one egress device and to each center stage device.

14. (Original): The switch element of claim 11, wherein the first ingress device includes a plurality of ingress routers, each ingress router selecting the ingress edge of one of the center stage devices for a time slot provided by one of the ingress data lines, each ingress router being assigned to only one ingress data line.

15. (Original): The switch element of claim 14, wherein a size of each ingress router is equal to the number of center stage devices.

16. (Original): The switch element of claim 14, wherein the first egress router includes a plurality of egress routers, each egress router selecting the egress edge of one of the center stage devices for a time slot provided by one of the egress data lines, each egress router being assigned to only one egress data line.

17. (Original): The switch element of claim 16, wherein a size of each egress router is equal to the number of center stage devices.

18. (Original): The switch element of claim 14, wherein more than one ingress router shares time slots with one ingress data line, but each ingress router is assigned to only ingress data line.

19. (Original): The switch element of claim 16, wherein more than one egress router shares time slots with one egress data line, but each egress router is assigned to only egress data line.

20. (Original): The switch element of claim 11, wherein the processor is configured to clear all existing traffic in order to connect the set of ingress lines to the set of egress lines.